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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,723	11/13/2002	Kevin A. Batson	FIS920010179	6157

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EXAMINER	
BAKER, STEPHEN M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,723	BATSON ET AL.	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-20* is/are allowed.

6)☒ Claim(s) *1-4,6-12,14-16,21,22,24 and 25* is/are rejected.

7)☐ Claim(s) *5,13,23 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-12, 14-16, 21, 22, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,796,662 to Kalter *et al* (hereafter "Kalter") in view of U.S. Patent No. 4,639,898 to Sauer (hereafter "Sauer").

Kalter discloses a wide-I/O DRAM chip with spare bitlines and a "coupling circuit" that "directly connects" adjacent first or second bitlines to a "data line" based on a "steering signal." In one embodiment (not shown) the first and second bitlines are adjacent bitlines (col. 9, lines 19-24), although Kalter indicates that such an embodiment is not the most efficient. The first bitline may still be used as a replacement for the adjacent bitline on the side opposite the second bitline. The potential of the first bitline is presumably maintained at a desired potential, although a means for maintaining bitline potential is apparently outside the scope of Kalter's description of bitline sparing logic.

Sauer discloses maintaining bitlines at a desired potential to improve the operation of a memory array. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate Sauer's bitline potential

maintaining means into Kalter's DRAM. Such incorporation would have been obvious because Sauer teaches that maintaining bitlines at a desired potential improves the operation of a memory array.

Regarding claims 2 and 10, Kalter shows more bitlines per column than the number of data lines, in the conventional manner.

Regarding claims 3 and 11, Kalter shows coupling one data line to one bitline, with a different bitline being coupled to each data line, in the conventional manner.

Regarding claims 4 and 12, Sauer's bitline potential maintaining is performed on failed bitlines.

Regarding claims 6 and 14, Kalter shows data lines to transfer data in parallel to the bitlines and bitlines coupled in parallel to plural memory cells, in the conventional manner.

Regarding claims 7 and 15, Kalter's data lines are "arranged in serial order" and each data line has a corresponding "means for coupling ... to corresponding respective second bitlines," in the conventional manner.

Regarding claims 8 and 16, Kalter's steering signals of course correspond to positions of failed bitlines.

Regarding claims 21 and 24, Kalter's sense amps serve as a "latch stage connected to a switch stage," in the conventional manner.

Regarding claims 22 and 25, Kalter teaches an "additional coupling circuit" as recited, to accommodate more than one spare.

3. Claims 1-4, 6-12, 14-16, 21, 22, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,796,662 to Kalter *et al* (hereafter "Kalter") in view of U.S. Patent No. 5,499,211 to Kirihata *et al* (hereafter "Kirihata").

Kalter discloses a wide-I/O DRAM chip with spare bitlines and a "coupling circuit" that "directly connects" adjacent first or second bitlines to a "data line" based on a "steering signal." In one embodiment (not shown) the first and second bitlines are adjacent bitlines (col. 9, lines 19-24), although Kalter indicates that such an embodiment is not the most efficient. The first bitline may still be used as a replacement for the adjacent bitline on the side opposite the second bitline. The potential of the first bitline is presumably maintained at a desired potential, although a means for maintaining bitline potential is apparently outside the scope of Kalter's description of bitline sparing logic.

Kirihata discloses maintaining bitlines at a desired potential to improve the operation of a memory array. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate Kirihata's bitline potential maintaining means into Kalter's DRAM. Such incorporation would have been obvious because Kirihata teaches that maintaining bitlines at a desired potential improves the operation of a memory array.

Regarding claim 4, Kirihata's bitline potential maintaining is performed on failed bitlines.

Allowable Subject Matter

4. Claims 17-20 are allowed.

5. Claims 5, 13, 23 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments with respect to claims 1-4, 6-12, 14-16, 21, 22, 24 and 25 have been considered but are moot in view of the new grounds of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen M. Baker
Primary Examiner
Art Unit 2133

smb